UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/275,726	03/24/99	DERVISOGLU	B 19705-000100

WM31/1031

LAW OFFICES OF GARY T. AKA
12930 SARATOGA AVENUE
SUITE D1
SARATOGA CA 95070

EXAMINER	
TON, D	
ART UNIT	**PAPER NUMBER**
2133	15

DATE MAILED: 10/31/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	Examiner	Group Art Unit	

—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication .
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

☑ Responsive to communication(s) filed on 8/10/01.

☑ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle,* 1935 C.D. 1 1; 453 O.G. 213.

Disposition of Claims

☑ Claim(s) 1-22 is/are pending in the application.

Of the above claim(s)____ is/are withdrawn from consideration.

☐ Claim(s)____ is/are allowed.

☑ Claim(s) 1-22 is/are rejected.

☐ Claim(s)____ is/are objected to.

☐ Claim(s)____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The proposed drawing correction, filed on____ is ☐ approved ☐ disapproved.

☐ The drawing(s) filed on____ is/are objected to by the Examiner.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119 (a)-(d)

☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 11 9(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number)____.

☐ received in this national stage application from the International Bureau (PCT Rule 1 7.2(a)).

*Certified copies not received:____.

Attachment(s)

☑ Information Disclosure Statement(s), PTO-1449, Paper No(s). 13

☑ Interview Summary, PTO-413

☑ Notice of Reference(s) Cited, PTO-892

☐ Notice of Informal Patent Application, PTO-152

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Other____

Office Action Summary

DETAILED ACTION

1. Applicant's Supplemental Amendment C filed on 08/10/01 has been reviewed.

2. Claims 1-22 are presented for examination.

3. Rajski and Gheewala (5,065,090 and 5,202,624) were cited as prior art in a previous Office Action.

Claim Rejections - 35 USC § 103

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. Claims 1-10 and 13-22 are rejected under 35 U.S.C. § 103(a) as being unpatentable over **Rajski et al.** (Rajski) patent no. **5,991,898**, in view of **Gheewala** patent no. **5,065,090**.

As per claims 1, 10 and 15:

Rajski teaches the invention substantially as claimed, including an integrated circuit [IC 10, Fig. 1] having logic blocks [CUT 14, Fig. 1] comprising:

a control unit [embedded processor core 12, Fig. 1] for performing test and debug operations of said logic blocks of said integrated circuit;

a memory [non-volatile memory 18, Fig. 1] associated with said control unit, said memory holding instructions for said control unit [col. 5 lines 50-60].

Rajski does not teach a plurality of probe lines responsive to said control unit for carrying system operation signals from predetermined probe points wherein said probe line comprises strings of storage elements providing signal paths from said probe point.

Gheewala teaches a cross-check test structure consists of serial/parallel shift registers with probe lines and sense lines to control the probe lines and to observe the output of the sense lines [Fig. 4 and col. 8 lines 21-56].

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the teachings of Rajski to provide a built in self test of multiple scan based integrated to have a test structure consists of shift registers with probe lines for controlling and observing the probe lines as taught by Gheewala. This modification would have been obvious and a person having ordinary skill in the art would have been motivated to do so because it would reduce the external probe points requirement to less than 10 compare to 200 probe points [see Gheewala col. 3 lines 66 - col. 4 lines 4].

As per claims 2 and 5:

Rajski teaches a plurality of scan lines [scan registers 16, Fig. 1] responsive to said control unit for loading test signals for said logic blocks and retrieving test signal results from said logic blocks, said test signals and said test signal results stored in said memory so that said loading and retrieving operations are performed to said integrated circuit [col. 4 lines 23-42].

As per claim 3:

Rajski teaches the integrated circuit further comprising a unit [data path 12, Fig. 5] coupled to said control unit and said memory, said unit testing said logic blocks and said memory responsive to and in cooperation with said control unit to self-test said integrated circuit.

As per claim 4:

Rajski teaches the integrated circuit wherein said scan lines comprise a first string of flip-flop [LFSR 50, Fig. 7] connectors connected between logic block and the remainder of said integrated circuit proximate said logic block [scan registers 16 connected between blocks CUT, Fig. 1], said flip-flop connectors providing signal paths between said logic block and the remainder of said integrated circuit proximate said logic block in one mode and carrying test signals and test signal results in a second mode [test mode 21, Fig. 2, claim 25, col. 19 begin at line 9].

As per claims 6-9:

Gheewala teaches probes lines comprises a string of programmable connectors providing a signal path for carrying system operation signal at predetermined probe points of said logic blocks [Fig. 2].

As per claims 13-4 and 16-22:

Gheewala et al. teaches each of said probe lines comprises a string of programmable connectors operating at one or more clock rates [Fig. 4 and col. 8 lines 21-56].

6. Claims 11-14 are rejected under 35 U.S.C. § 103(a) as being unpatentable over **Rajski et al.** (Rajski) patent no. **5,991,898**, in view of **Gheewala** patent no. **5,065,090** and further in view of **Gheewala et al.** patent no. **5,202,624**.

As per claims 11 and 12:

Rajski and Gheewala (5,065,090) do not teach an IC including a trigger logic.

Gheewala et al. (5,202,624) teaches a trigger logic [see circuitry of Fig. 3 and the logic of TABLE A on col. 6 and TABLE B on col. 8] responsive to said system operation signals for initiating/terminating storage of said system operation signals in said memory [when P1=0 and P2=0, S2 value is written into latch 68, when control signal C=1, the value then transmitted to driver 42, col. 7 lines 1-15].

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Rajski and Gheewala to include a trigger logic for initiating/terminating storage of said system operation signals in said memory as taught by Gheewala et al. because it would provide the advantages that the test signals are loaded to internal probe points without the need for complex scan registers [see Gheewala et al. col. 2 lines 42-57].

Response to Arguments

7. Applicant argues that the prior art of record do not teach the probe lines comprises string of storage element providing signal paths from said probe points.

The newly cited art, Gheewala, teaches a cross-check test structure consists of serial/parallel shift registers with probe lines for providing signal paths from a probe point by controlling the parallel/serial control 29 and the clock 30 [Fig. 4 and col. 8 lines 21-56].

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the teachings of Rajski to provide a built in self test having a cross-check test structure consists of string of shift registers with probe lines for providing signal paths from a probe

point as taught by Gheewala. This modification would have been obvious and a person having ordinary skill in the art would have been motivated to do so because it would reduce the external probe points requirement to less than 10 compare to 200 probe points [see Gheewala col. 3 lines 66 - col. 4 lines 4].

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for response to this final action is set to expire THREE MONTHS from the date of this action. In the event a first response is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event will the statutory period for response expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Ton, whose telephone number is (703) 306-3043. The examiner can normally be reached Monday through Thursday from 6:30 AM to 4:00 PM and alternate Friday from 6:30 AM to 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady, can be reached at (703) 305-9595.

Any inquiry of a general nature of relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to: (703) 746-7239 (Official)

(703) 746-7240 (Non-Official)

(703) 746-7238 (After-Final)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

David Ton

Patent Examiner

October 29, 2001